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55. (Amended) A system for performing address translations comprising:

a virtual to linear address converter circuit for generating a calculated linear address based on a virtual address, said virtual address having both a segment identifier and a segment offset, and said calculated linear address being based on all of said virtual address; and

a linear to physical address converter circuit for generating a calculated physical address based on the calculated linear address, the calculated physical address including a calculated page frame and a calculated page offset; and

a fast physical address circuit for generating a fast physical address including a fast page frame and a fast page offset;

wherein a memory reference can be generated based on the fast physical address;

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[The system of claim 54,] further wherein the fast physical address is based on linear address information relating to the virtual address and physical address information relating to a prior virtual address.

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56. (Amended) A system for performing address translations comprising:

a virtual to linear address converter circuit for generating a calculated linear address based on a virtual address, said virtual address having both a segment identifier and a segment offset, and said calculated linear address being based on all of said virtual address; and

a linear to physical address converter circuit for generating a calculated physical address based on the calculated linear address, the calculated physical address including a calculated page frame and a calculated page offset; and

a fast physical address circuit for generating a fast physical address including a fast page frame and a fast page offset,

wherein a memory reference can be generated based on the fast physical address;

[The system of claim 54,] further wherein the virtual address is partially converted to a linear address by the fast physical address circuit and is combined with physical address information relating to a prior virtual address to generate the tentative physical address.

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81. (Twice amended) A system for performing address translations using a first operation to convert a first virtual address having both a segment identifier portion and a segment offset portion to a first linear address, such that all portions of the virtual address are considered when converting said virtual address into the first linear address and a second operation to convert said first linear address to a first physical address, the system further including:

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an address translation memory, accessible by said system while said first operation is converting said first virtual address, and capable of storing prior physical address information generated during a prior address translation by said second operation based on a prior virtual address;

wherein a fast physical address can be generated based on the prior physical address information and said first linear address before said second operation has completed converting said first linear address to the first physical address.

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82. (Twice amended) A system for performing memory references in a processor which employs both segmentation and optional independent paging during an address translation, said system comprising:

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means for performing an address translation by generating a first physical address from a first virtual address by first calculating a first linear address based on both a first segment identifier and first offset associated with the first virtual address, such that all of said first virtual address is translated, and then calculating the first physical address based on the first calculated linear address; and

a fast physical memory access circuit for generating a fast memory reference, which fast memory reference is based on physical address information from said means for performing an address translation [means];

a bus interface circuit for initiating a fast memory access to a memory subsystem based on said fast memory reference.

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